



JPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application

Inventors: Osamu ICHIKAWA

Application No.: 10/647,506

Filed: August 26, 2003

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND MEMORY TEST METHOD

STATUS INQUIRY LETTER

Assistant Commissioner of Patents
Washington, DC 20231

Sir:

It would be appreciated if you would indicate the status of the above identified application, including a written indication as to when the next communication can be expected.

Respectfully submitted,

James E. Ledbetter
Registration No. 28,732

Date: October 25, 2004

JEL/ejw

Attorney Docket No. L8462.03109

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